# A MONOLITHIC SI PCS-CDMA POWER AMPLIFIER WITH AN IMPEDANCE-CONTROLLABLE BIASING SCHEME

Sifen Luo and Tirdad Sowlati

Philips Research, Briarcliff Manor, New York 10530, USA

***Abstract* — This paper for the first time presents a monolithic Si PCS-CDMA power amplifier (PA) capable of delivering 28.2dBm output power with 30% power-added efficiency (PAE) and –45dBc adjacent-channel-power ratio (ACPR) at 1.9GHz and 3.6V supply voltage. The PA implemented in a 30GHz BiCMOS process incorporates a novel impedance-controllable biasing scheme to control class of operation and bias impedance of the output stage.**

## I. INTRODUCTION

Monolithic RF PAs for mobile-phone handset applications have traditionally been the territory of GaAs technologies. Efforts have been made on designing nonlinear PAs [1]-[2] at both the cellular frequency (900MHz) band and the PCS frequency (1.9GHz) band using Si technologies. Recently, high-efficiency linear PAs were demonstrated at the above two bands using SiGe HBT technologies [3]-[4]. The PA for the CDMA applications at the lower band could deliver 28dBm output power with 36% PAE and –44.1dBc ACPR [3], while the CDMA PA at the higher band could deliver 30dBm output power with 41% PAE and –46dBc ACPR [4]. However, the latter was still a hybrid solution. Si monolithic RF PAs have advantages in low cost and ease of integration with other mainstream Si-based circuits. To date, no monolithic Si PCS-CDMA PA has been reported yet.

The modulation scheme of the CDMA system requires the PA used in the handset to be highly linear. This makes it very challenging to design a monolithic PCS-CDMA PA with high efficiency using Si technologies due to their inherently high substrate loss and parasitics.

A monolithic Si PCS-CDMA PA capable of delivering 28.2dBm output power with 30% PAE, -45dBc ACPR, and 21.5dB gain at 1.9GHz and a supply voltage of 3.6V is demonstrated for the first time in this paper. The PA was mounted chip-on-board (COB) with low-cost surface-mount components for both input and output matching networks. The results were obtained from an FR-4 test board using a 50Ω measurement system.

In Section II, a conventional biasing scheme for the output stage of the PA is discussed. Then, an impedance-controllable biasing scheme for the PA and its advantages over the conventional one are presented in Section III. Measured results of the PA with the impedance-controllable biasing scheme are given in Section IV. Finally, a conclusion is drawn in Section V.

## II. CONVENTIONAL BIASING SCHEME

Fig. 1 shows a simplified schematic of a PA consisting of two common-emitter stages (Q0 and Q1). The output-matching network consists of capacitors C3 to C5, inductors L2, and two transmission lines (CPWs). The input matching network consists of capacitors C6 and C7 and a transmission line (CPW). The input stage is biased through an on-chip resistor Rb1 using a bias voltage Vb1 for simplicity. A conventional current-mirror circuit comprised of Q2 and Q3 is used to bias the output stage.

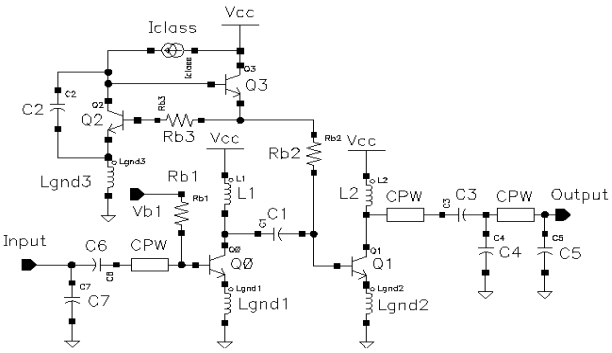


Fig. 1 Schematic of the PA with a conventional biasing scheme.

In Fig.1, Lgnd1, Lgnd2 and Lgnd3 are ground inductors from bonding wires. L1 and L2 are off-chip inductors. The interstage-matching network consists of an on-chip capacitor C1 and L1 realized using a bonding wire and a PCB trace. C2 is an on-chip bypass capacitor.

This biasing scheme for Q1 provides a near-constant small-signal impedance (1MHz) presented at the base of Q1 and a nearly linear control of the collector's quiescent current of Q1 as shown in Fig. 2 with Rb2=15Ω. When

Q0 and Q1 are biased into class AB operation, however, its large-signal impedance presented at the base of Q1 at 1.9GHz is capacitive and much larger than its small-signal counterpart as shown in Fig. 3, where the PA's output power versus input signal levels is also shown. It is seen that the PA starts to saturate at the output power close to 600mW. This is due to the fact that as the output power increases, the average voltage drop across the bias impedance increases. This causes a reduction in the base-emitter voltage of Q1 and thus pushes it into saturation [5].

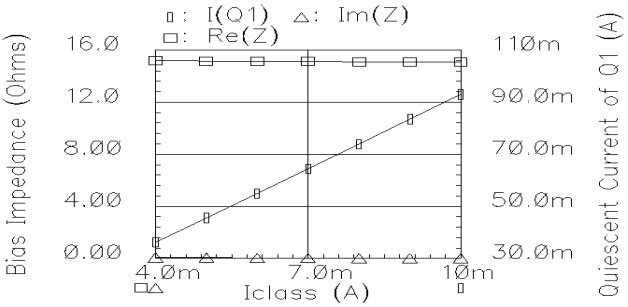


Fig. 2 Quiescent current of Q1 and small-signal impedance (1MHz) of the conventional biasing scheme as functions of Iclass (Rb2=15Ω).

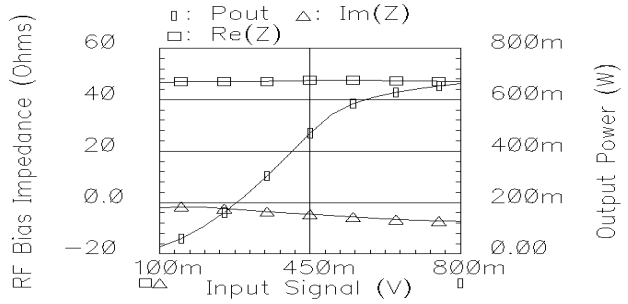


Fig. 3 RF impedance of the conventional biasing scheme and output power of the PA as functions of the input signal level (Rb2=15Ω, Iclass=8mA).

## III. Impedance-Controllable Biasing Scheme

Fig. 4 shows a simplified schematic of a PA using an impedance-controllable biasing scheme to bias Q1 [6]. It is identical to the PA shown in Fig. 1 except for the biasing scheme for Q1. The biasing scheme is comprised of two current-mirror subcircuits: one consisting of transistors Q2, Q4 and Q7 and the other consisting of transistors Q5 and Q6. This biasing scheme is capable of providing independent control of bias impedance and class of operation of Q1 by properly choosing Iclass and Ibias. Whereas Ibias controls the output impedance of the bias circuit, Iclass controls the quiescent current of the output stage. This proposed biasing scheme allows the output stage to be adjusted for optimum efficiency and linearity.

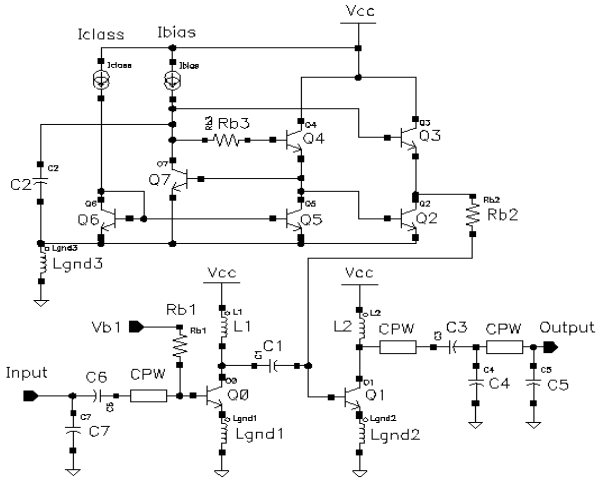


Fig. 4 Schematic of the PA with an impedance-controllable biasing scheme.

The mechanism of its controlling the quiescent current is explained below. Neglecting base currents, we have

$$V_{be}(Q1)+V_{be}(Q3)+V(R_{b2})=V_{be}(Q2)+V_{be}(Q4)+V(R_{b3}) \quad (1)$$

and since Q2 and Q3 have the same current, we then have

$$V_{be}(Q3)=V_{be}(Q2). \quad (2)$$

This leads to

$$V_{be}(Q1)=V_{be}(Q4) \quad (3)$$

when

$$V(R_{b2})=V(R_{b3}) \quad (4)$$

by properly choosing Rb2 and Rb3. The current flowing in Q6 must flow in Q5 and Q4 because Q5 and Q6 form a current mirror. Since Iclass controls the current flowing in Q6, therefore it dictates the quiescent current in Q4 that in turn controls the quiescent current in the output transistor Q1. The mechanism of Ibias's controlling the output impedance of the biasing circuit can be explained in a similar fashion. By properly scaling the emitter area ratios between transistor pairs, one can readily control the quiescent current of the output stage and the output impedance of the bias circuit. This helps to optimize the efficiency of the output stage while maintaining the required linearity.

The collector's quiescent current of Q1 and low-frequency (1MHz) small-signal impedance of the impedance-controllable biasing scheme presented at the base of the output stage as functions of Iclass and Ibias are shown in Figs. 5 and 6. For simplicity, Rb3 is set to zero (Rb3=0) in this analysis. It is seen that the control current Iclass in both biasing schemes has a similar effect on the quiescent current of Q1 and the bias impedance: near-constant bias impedance and nearly linear control of the quiescent current. Furthermore, the control current Ibias provides an additional means to adjust the bias impedance and only slightly changes the quiescent current.

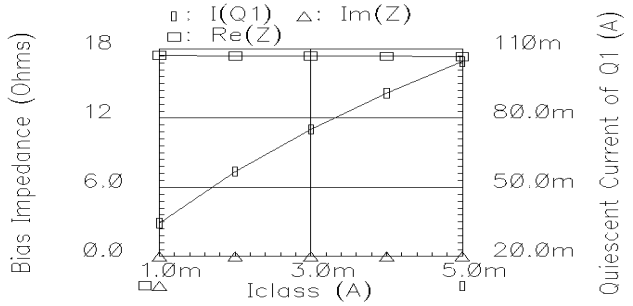


Fig. 5 Quiescent current of Q1 and small-signal impedance (1MHz) of the impedance-controllable biasing scheme as functions of Iclass (Rb2=15Ω , Ibias=3mA).

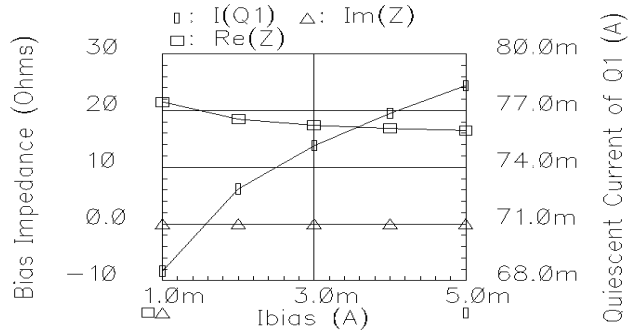


Fig. 6 Quiescent current of Q1 and small-signal impedance (1MHz) of the impedance-controllable biasing scheme as functions of Ibias (Rb2=15Ω and Iclass=3mA).

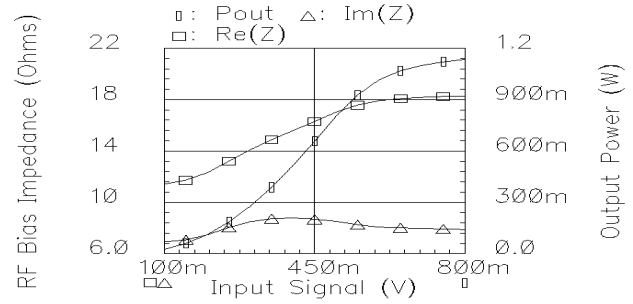


Fig. 7 RF impedance of the impedance-controllable biasing scheme and output power of the PA as functions of the input signal level (Rb2=15Ω, Iclass=Ibias=3mA).

It is of more interest to see its large-signal impedance presented at the base of Q1 at 1.9GHz. Fig. 7 shows the RF impedance of the impedance-controllable biasing scheme and the output power as a function of the input signal level. For a fair comparison, the sizes of Q0 and Q1 and the bias conditions have been set identical to those for the PA discussed in Section II. There are several advantages of using the impedance-controllable biasing scheme. Firstly, it presents low impedance at the base of Q1. Secondly, its large-signal impedance is inductive and not far off from its low-frequency small-signal values. This helps interstage matching by canceling part of the capacitive base impedance of Q1. Thirdly, it helps increase output power due to its low RF impedance. As seen in Fig. 7, the PA only starts to saturate at the output power close to 1W. This is a significant improvement over that of the PA with the conventional biasing scheme.

The PA was simulated using Cadence's SpectreRF and Agilent Technologies' Circuit Envelope Simulator. A CDMA input signal was used in the circuit envelope simulation. The impedance-controllable biasing scheme allowed the PA to achieve the required ACPR with efficiency higher than 30%.

## IV. Measured Results

The PA with the impedance-controllable biasing scheme was implemented in a Philips BiCMOS process (QUBiC3) featuring 30GHz ft NPNs, 0.5μm CMOS and high value poly resistors. The emitter area of Q1 is 128x0.7μmx20.2μm. A photomicrograph of the die with an area of about 0.9 $mm^2$ is shown in Fig. 8.

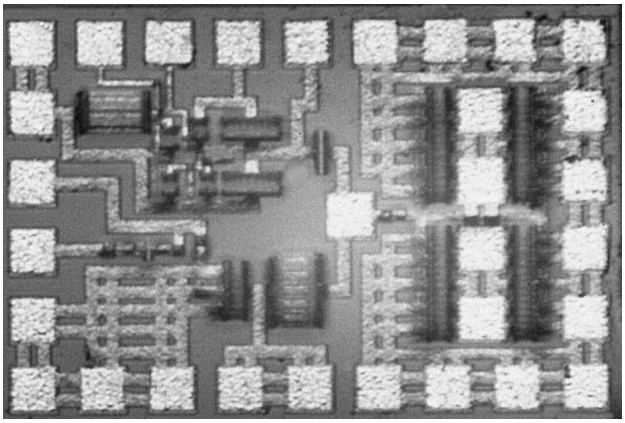

Fig. 8 Photomicrograph of the die.

The PA was first tested at 1.9GHz using a three-stub tuner in the output for benchmarking its performance. Both the input and output stages were biased in a class AB operation. The PA's ACPR and PAE versus the output power are shown in Fig. 9. A spectrum analyzer from Rohde & Schwarz was used in the ACPR measurements. With the output matched using the tuner, the PA delivers 28.1dBm output power with 24.5dB gain, 31.5% PAE and –45dBc ACPR. It is worth noting that in this PA, there is a valley with a quite steep slope in the ACPR curve. This indicates that one can improve ACPR margins with a slight back-off from the highest output power level.

The tuner was then replaced by surface-mount components on the FR-4 test board. The PA was again tested at 1.9GHz with a slightly lower base bias voltage for the input stage to enhance its PAE. Iclass and Ibias were

readjusted to compensate drops in PAE and gain due to the insertion loss from the surface-mount components. The PA's ACPR and PAE versus the output power are shown in Fig. 10. With the input and output matching networks using the low-cost surface-mount components on the FR-4 test board, the PA delivers 28.2dBm output power with 21.5dB gain, 30% PAE and –45dBc ACPR. The same steep slope can be seen in the ACPR curve near the peak output power level. At lower output power levels, there is a peak almost reaching the ACPR limit (-45dBc) in the ACPR curve due to the lower bias in the input stage.

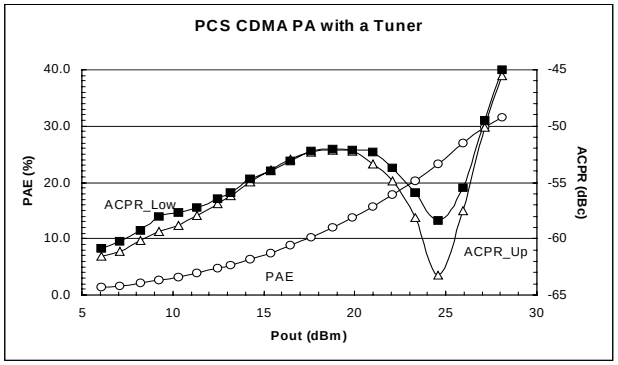


Fig. 9 Measured ACPR and PAE of the PA with the tuner.

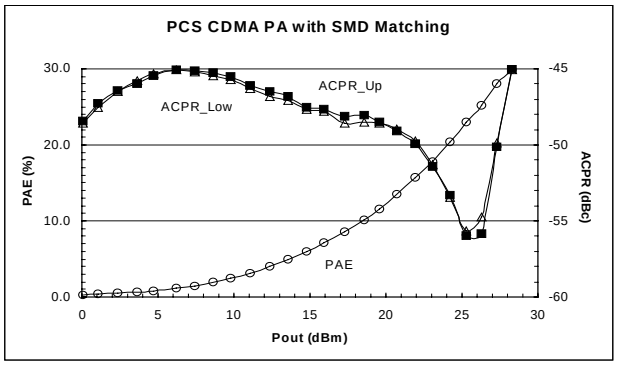


Fig. 10 Measured PAE and ACPR of the PA with matching networks using the surface-mount components.

Fig. 11 shows an actual ACPR measurement of the PA matched with the surface-mount components at its highest linear output power level. A 10dB attenuator and a coaxial cable were used in the output. Their combined measured attenuation is 10.8dB. This attenuation plus the reading of 17.45dBm channel power adds up to 28.25dBm output power. It is seen that whereas the ACPR reaches its specified limit of -45dBc, the alternate-channel-power ratio has large margins over its specification of –56dBc. The effectiveness of the impedance-controllable biasing scheme has been verified in these measurements.

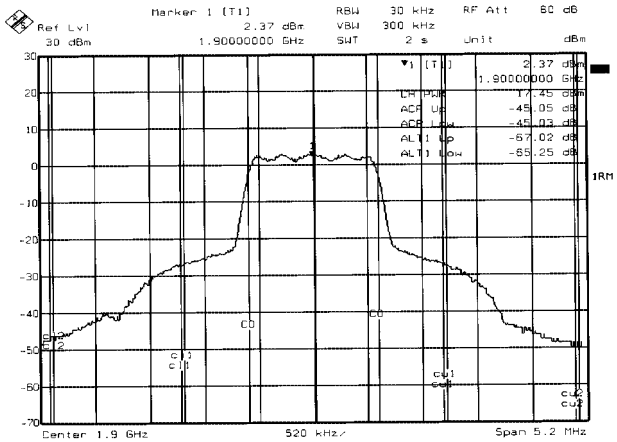


Fig. 11 A snapshot of the ACPR measurement of the PA with the matching networks using surface-mount components.

## V. Conclusion

A Si PCS-CDMA PA with a novel impedance-controllable biasing scheme, mounted COB and matched with low-cost surface-mount components, is demonstrated for the first time capable of delivering 28.2dBm output power with 30% PAE, -45dBc ACPR, and 21.5dB gain at 1.9GHz and 3.6V supply voltage.


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## References


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